REMARKS

By this amendment claims 1, 3, 6, and 11 have been amended and claims 13-18 have been added. Claims 1-18 remain pending. Reconsideration of the application as amended is respectfully requested.

Rejections under 35 USC §112

Claims 3-5 have been rejected under 35 USC §112 as depending from an nonexistent claim. Claim 3 has been amended to correct the deficiency, which overcomes the Examiner's rejection under 35 USC §112.

Rejections under 35 USC §102(e)

Claims 1, 2, and 6-12 have been rejected under 35 USC §102(e) over Tang, et al. (US 6,507,064). Tang describes a semiconductor device comprising a wafer 12, contact pads 34, 38, a digit line portion 62 contacting pad 38, a capacitor storage node 82 contacting pad 34, a cell dielectric layer 92, and a dielectric spacer 54 which contacts the digit line portion 62 and the cell dielectric layer 92, with the cell dielectric layer 92 contacting the storage node 82. Tang uses insulating spacers 54 to function as an etch stop during an etch of layer 52 (col. 5 lines 23-27).

The rejected claims as amended comprise novel and nonobvious differences over Tang. Claim 1, for example, recites a semiconductor device comprising "...a digit line contact plug portion [which] contacts the first contact pad...a capacitor storage node...and a dielectric layer interposed between the digit line contact plug portion and the capacitor storage node, and which contacts both the digit line contact plug portion and the capacitor storage node." This is novel and nonobvious over Tang. For example, FIG. 9 of Tang depicts a plug portion 62 and a capacitor storage node 82, and at least two interposed dielectric layers 54 and 92, neither of which contacts both the digit line contact plug portion 62 and the storage node 82. As depicted in FIG. 7, Tang intentionally forms dielectric spacer 54 so that it does not contact storage node 82 and removes all intervening layers to provide a double sided container capacitor. Thus Tang teaches away from interposing a dielectric layer between the plug portion 62 and the storage node 82, and which contacts both, as the formation process of Tang is not conducive to forming, and does not provide, the structure presently claimed. Thus claim 1 and rejected claim 2 which depends therefrom are allowable over Tang under 35 USC §102(e).

Claim 6 has been amended to include the recitation "...a dielectric layer interposed between the contact plug and each of the first and second spaced capacitor storage plates, wherein the dielectric layer contacts each of the first and second spaced capacitor storage plates and the contact plug." Independent claim 11 recites a similar feature, specifically "...a second dielectric layer; a first portion of a digit line contact plug within and contacting the second dielectric layer and electrically coupled with the contact pad; [and] a capacitor storage node within and contacting the second dielectric layer...".

As discussed relative to the rejection of claim 1, Tang neither teaches nor suggests such a structure. Thus rejected independent claims 6 and 11, and rejected claims 7-10 and 12 which depend therefrom, are allowable over Tang for at least this reason.

With regard to claim 12, the Examiner at the first full paragraph on page 3 states that Tang teaches a spacer as part of the insulating layer (102) which is positioned between the top plate (94) and the second portion of the digit line contact (106). These structures are depicted at FIG. 9 of Tang, for example.

It is submitted that this portion of insulating layer 102 is not properly referred to as a "spacer" as commonly used in the art of semiconductor manufacture. A spacer is typically formed as a blanket layer over a topographical feature which provides a sidewall, then the blanket layer is anisotropically etched, for example using a vertical etch, to remove the layer from horizontal features and leaving portions of the layer over the sidewall. In fact, Tang itself does not refer to structure 102 discussed by the Examiner as a "spacer" but as a "thick insulation layer" having a patterned bit line contact via (col. 6 lines 37-44). Tang does teach spacers as commonly used in the art of semiconductor manufacture, for example elements 16 and 54, and does refer to these structures repeatedly throughout the document as "spacers" (see col. 4 line 54 and numerous instances at col. 5 line 18 - col. 7 line 9). It is therefore submitted that the Examiner's use of the specified portion of layer 102 to teach a "spacer" is inappropriate, as falling well outside the typical meaning of a "spacer" as used in the art of semiconductor manufacture. Thus the Examiner's use of the specified portion of layer 102 to teach the spacer of the present invention as recited in claim 12, which is applied according to common usage in the art of semiconductor manufacture, is respectfully traversed.

Rejected claims 1, 2, and 6-12 as amended are therefore allowable over Tang under 35 USC §102(e).

Newly-added claims

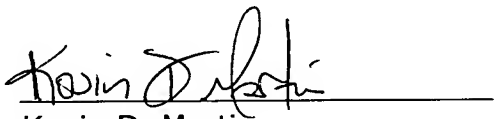
Claims 13-15 recite the structure of claims 1, 6, and 11 respectively, and further include that a "majority of a thickness of the dielectric layer is interposed between the digit line contact plug portion and the capacitor storage node" (claim 13) or a similar recitation appropriate for each independent claim. As Tang fails to teach or suggest such a structure, these claims are further allowable over Tang.

Claim 16 recites "...a spacer having a first portion which contacts the capacitor top plate and which is recessed within an opening defined by the dielectric layer and the capacitor dielectric layer and further having a second portion which is not recessed within the opening. Tang does not appear to teach or suggest a spacer recessed within such an opening.

Conclusion

The claims are therefore believed to be in condition for allowance. If there are matters which may be clarified through a telephone call, the Examiner is cordially invited to call the undersigned. This is believed to be a complete response to the Examiner's rejection.

Respectfully submitted,



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